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CLAIMS

1. A method of making a via of a semiconductor device, comprising:

forming a dielectric layer on a metallic layer;

forming a via hole through the dielectric layer to expose a surface portion of the metallic layer;

forming a titanium aluminide layer on the exposed surface portion; and

depositing a conductive material on the titanium aluminide layer.

2. The method as recited in claim 1, further comprising providing a substrate supporting the metallic layer.

3. The method of claim 1, further comprising providing a substrate supporting the metallic layer and a passivation layer on the substrate prior to the forming of the metallic layer, wherein the metallic layer if formed directly on the passivation layer.

4. The method as recited in claim 1, further comprising forming a further metallic layer on the dielectric and electrically connected to the conductive material.

5. The method as recited in claim 1, wherein the forming of the titanium aluminide layer comprises forming a $TiAl_3$ layer.

6. The method as recited in claim 1, further comprising forming the metallic layer as an aluminum layer prior to the forming of the dielectric layer.

7. The method as recited in claim 6, wherein the aluminum layer comprises an aluminum alloy.

8. The method as recited in claim 1, wherein the conductive material comprises a titanium compound layer.

9. The method as recited in claim 1, wherein the conductive material comprises a titanium nitride layer, and further comprising depositing a refractory metal plug on the conductive material.

10. The method as recited in claim 1, wherein the conductive material comprises an aluminum plug.

11. A method of making a via of a semiconductor integrated circuit device, comprising:
forming a dielectric layer on an aluminum layer;
forming a via hole through the dielectric layer to expose a surface portion of the aluminum layer at a bottom of the via hole;
forming a titanium aluminide layer on the exposed surface portion;
forming a titanium nitride layer on the titanium aluminide layer; and
depositing tungsten on the titanium nitride layer by reduction of tungsten hexafluoride.

12. A method of making a via of a semiconductor integrated circuit device, comprising:
forming a dielectric layer on an aluminum layer;
forming a via hole through the dielectric layer to expose a surface portion of the aluminum at a bottom of the via hole;
depositing a titanium aluminide layer on the exposed surface portion; and
depositing a conductive material on the titanium aluminide layer.

13. The method as recited in claim 12, wherein the depositing of the titanium aluminide layer comprises sputter depositing the titanium aluminide.

14. The method as recited in claim 12, wherein the depositing further deposits titanium aluminide on sidewalls of the via hole.

15. The method as recited in claim 12, wherein the depositing of the titanium aluminide comprises depositing $TiAl_3$.

16. The method as recited in claim 12, wherein the conductive material comprises a titanium nitride layer, and further comprising depositing a refractory metal plug on the conductive material by reduction of a refractory metal halide compound.

17. A method of making a via of a semiconductor integrated circuit device, comprising:
forming a dielectric layer on an aluminum layer;
forming a via hole through the dielectric layer to expose a surface portion of the aluminum layer at a bottom of the via hole;
depositing a titanium layer on the exposed surface portion;
heating the titanium layer to form titanium aluminide; and
depositing a conductive material on the titanium aluminide layer.

18. The method as recited in claim 17, wherein the heating to form titanium aluminide occurs concurrent with the depositing of the titanium film.

19. The method as recited in claim 17, wherein the heating to form titanium aluminide occurs after the depositing of the titanium film and prior in time to the depositing of the conductive material.

20. The method as recited in claim 17, wherein the depositing of titanium further deposits titanium on sidewalls of the via hole.

21. The method as recited in claim 17, wherein the depositing of the titanium aluminide comprises depositing $TiAl_3$.

22. The method as recited in claim 17, wherein the heating of the titanium layer results in at least substantially all of the titanium layer being consumed by a reaction with the aluminum layer to form the titanium aluminide layer.

23. The method as recited in claim 17, wherein the conductive material comprises a titanium nitride layer, and further comprising depositing a refractory metal plug on the conductive material by reduction of a refractory metal halide compound.

24. A method of fabricating a semiconductor integrated circuit device comprising the steps of:

forming a circuit device region in a semiconductor substrate;

forming a first dielectric layer over the circuit device region;

forming an aluminum interconnection layer on the first dielectric layer over the circuit device region;

opening a contact hole through a first portion of the aluminum interconnection layer and the first dielectric layer;

forming a contact interconnect in the contact hole;

forming a second dielectric layer over the aluminum interconnection layer and the contact interconnect;

forming a via hole through the second dielectric layer exposing a first surface portion of the aluminum interconnection layer at the bottom of the via hole;

forming a titanium aluminide layer on the first surface portion;

depositing a titanium nitride layer on the titanium aluminide layer;

depositing a tungsten plug on the titanium nitride;

planarizing the tungsten plug; and

forming a metallic interconnection layer on the second dielectric layer and electrically connected to the planarized tungsten plug.

25. The method as recited in claim 24, further comprising the step of annealing the device after the forming of the metallic interconnection layer.

26. A semiconductor device, comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide liner.

27. A semiconductor device, comprising:
an aluminum layer over a substrate;
a dielectric layer on the aluminum layer;
a via hole extending through the dielectric layer to a surface of the aluminum layer;
a titanium aluminide layer lining at least a bottom of the via hole;
a titanium nitride layer substantially free of through cracks formed on the titanium aluminide;
a conductive plug material on the titanium nitride layer; and
a metallic layer on the dielectric layer and electrically connected to the plug material.

28. A semiconductor memory device, comprising:
a memory circuit region in a semiconductor substrate;
a first dielectric layer over the memory circuit region;
a first metallic layer over the first dielectric layer;
a contact interconnect between the first metallic layer and the substrate;
a second dielectric layer on the first metallic layer;
a via hole extending through the second dielectric layer to a surface of the second metallic layer;
a titanium aluminide layer lining at least a bottom of the via hole;
a titanium compound layer formed on the titanium aluminide;
a conductive plug material on the titanium compound layer; and
a second metallic layer on the second dielectric layer and electrically connected to the plug material.

29. The semiconductor memory device as recited in claim 28, wherein the titanium compound layer is titanium nitride.

30. The semiconductor memory device as recited in claim 28, wherein the first metallic layer comprises aluminum.

31. The semiconductor memory device as recited in claim 28, wherein the memory circuit includes a SRAM cell.

32. The semiconductor memory device as recited in claim 28, wherein the memory circuit includes a DRAM cell.

33. A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

a via hole extending through the dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

34. A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide liner; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

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35. A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

36. A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

a via hole extending through the second dielectric layer to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

37. A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

a via hole extending through the dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material.

38. A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide liner.

39. A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

40. A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

a via hole extending through the second dielectric layer to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.